REMARKS

Applicants appreciate the Examiner's thorough consideration provided the present application. Claims 1, 2, 4 and 6-15 are now present in the application. Claims 1, 4, 6 and 7 have been amended. Claims 14 and 15 have been added. Claims 3 and 5 have been cancelled. Claims 1 and 8 are independent. Reconsideration of this application, as amended, is respectfully requested.

Claim Rejections Under 35 U.S.C. §§ 102 & 103

Claims 1-4 and 7-11 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Wu, U.S. Patent No. 7,047,348. Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of Tsai, U.S. Patent No. 6,751,754. Claims 12 and 13 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Wu in view of Tsai, and further in view of Landry, U.S. Patent No. 6,732,301. These rejections are respectfully traversed.

In light of the foregoing amendments, Applicants respectfully submit that these rejections have been obviated and/or rendered moot. As the Examiner will note, independent claim 1 has been amended.

Independent claim 1 recites "controlling the access to the data stored in the buffer of debug card by means of a data control chip of the debug card, the step of controlling the access to the data stored in the buffer of debug card comprising: initializing the data control chip; if the data control chip is in an idle status, setting the data control chip wherein the step that if the data control chip is in an idle status setting the data control chip further comprising: setting a data access mode of the data control chip; determining a data access situation of the debug card and

performing counting; setting an amount of data to be accessed each time; and ending the idle status; and if the data control chip is not in an idle status, accessing to the PCI bus data stored in the debug card according to the settings of the data control chip."

Independent claim 8 recites "a PCI interface operable as a connecting interface with a PCI bus; a storage module for storing PCI bus data; and a data control chip operable to control the access and transmission of PCI bus data, the data control chip including: an access control module for controlling data access according to a control signal; a transmission control module for controlling data transmission according to a control signal; a data storage module for storing PCI bus data obtained from the debug card; a register for storing an access control command; and a host interface operable as an interface with a host."

Applicants respectfully submit that the above combinations of steps and elements as set forth in independent claims 1 and 8 are not disclosed nor suggested by the references relied on by the Examiner.

Wu is directed to a method and architecture for accessing hardware devices in computer system and chipset thereof, and discloses a SMB master controller serves as a SMB master device for generating a clock signal and transmitting a data signal defined by the SMB protocol to the system controller according to the clock signal, and a SMB slave controller serves as a SMB slave device for receiving commands and data bytes in the data signal from the SMB master device to drive the PCI master to access the register block of peripherals and system memory of the computer system. However, the SMB master controller and its function are different from the present application.

Unlike Wu, the present application discloses solutions such as: (a) controlling the access to the data stored in the buffer of debug card by means of a data control chip of the debug card, the controlling step comprises: initializing the data control chip; (b) setting the data control chip if the data control chip is in an idle status, wherein the setting step further comprises setting a data access mode of the data control chip; determining a data access situation of the debug card and performing counting; setting an amount of data to be accessed each time; and ending the idle status; and (c) accessing to the PCI bus data stored in the debug card according to the settings of the data control chip if the data control chip is not in an idle status. These claimed features are clearly absent from Wu.

With regard to the Examiner's reliance on the secondary references, these references have only been relied on for their teachings related to some dependent claims. These references also fail to disclose the above combinations of steps and elements as set forth in independent claims 1 and 8. Accordingly, these references fail to cure the deficiencies of Wu.

Accordingly, none of the references utilized by the Examiner individually or in combination teach or suggest the limitations of independent claims 1 and 8 or their dependent claims. Therefore, Applicants respectfully submit that independent claims 1 and 8 and their dependent claims clearly define over the teachings of the references relied on by the Examiner.

Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102 & 103 are respectfully requested.

Additional Claims

Additional claims 14 and 15 have been added for the Examiner's consideration. Applicants respectfully submit that claims 14 and 15 are allowable due to their respective dependence on independent claim 1, as well as due to the additional recitations included in these claims. Favorable consideration and allowance of additional claims 12-19 are respectfully requested.

CONCLUSION

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but merely to show the state of the prior art, no further comments are necessary with respect thereto.

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Joe McKinney Muncy, Registration No. 32,334 at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: March 14, 2007

Respectfully submitted,

By _____
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